



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

09/928,988

08/15/2001

Jun Koyama

740756-2348

8058

31780

7590

08/26/2004

ERIC ROBINSON

PMB 955

21010 SOUTHBANK ST.

POTOMAC FALLS, VA 20165

EXAMINER

NGUYEN, CHANH DUY

ART UNIT

PAPER NUMBER

2675

10

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/928,988

Applicant(s)

KOYAMA ET AL.

Examiner

Chanh Nguyen

Art Unit

2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 June 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 and 12-29 is/are pending in the application.
- 4a) Of the above claim(s) 7-9, 13 and 16-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6, 10, 12, 14 and 15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Amendment***

1. The amendment filed on June 03, 2004 and terminal disclaimer filed on June 14, 2004 have been entered and considered by examiner.

### ***Priority***

2. It is noted that this application appears to claim subject matter disclosed in prior Application No. 09/150,933, filed September 10, 1998. A reference to the prior application must be inserted as the first sentence of the specification of this application or in an application data sheet (37 CFR 1.76), if applicant intends to rely on the filing date of the prior application under 35 U.S.C. 119(e) or 120. See 37 CFR 1.78(a). For benefit claims under 35 U.S.C. 120, the reference must include the relationship (i.e., continuation, divisional, or continuation-in-part) of all nonprovisional applications. Also, the current status of all nonprovisional parent applications

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-6 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by applicant's admitted prior art (Figures 5 and 6).

Applicant's admitted prior art (Figures 5 and 6) discloses the most closely resembling the subject matter of the claims including thin film transistor, clock lines, two layer structures and black matrices as recited in the claims.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 10, 12 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over prior art admitted by applicant in view of Watanabe et al (U.S. Patent No. 5,815,223).

As to claim 10, note the discussion of prior art above, prior art admitted by applicant discloses a semiconductor as recited in claim 10 with exception that the prior art does not mention shielding line. Mitra teaches a well-known shielding line (103)

Art Unit: 2675

disposed on interval between the clock lines (101). Therefore, it would have been obvious to one of ordinary skill in the art at the invention was made to have used shielding line as taught by Mitra to the semiconductor of the prior art so as to help prevent clock signals propagated on the clock line from electromagnetically coupling with other signal lines .

As to claims 12 and 14-15, the limitations recited in these claims are met by the prior art admitted by applicant (Figures 5-6).

### ***Response to Arguments***

8. Applicant's arguments filed June 03, 2004 have been fully considered but they are not persuasive.

On page 7, last two paragraph, applicant argues that the Office Action has not established an anticipation rejection, Examiner disagree with applicant this point of view since the prior art (Figures 5 and 6) discloses the all the claimed limitation including thin film transistor, clock lines, two layer structures and black matrices as recited in the claims.

On page 8, applicant argues that "Figures 5 and 6 do not teach that each of clock lines or each of base portions of the clock lines is made of a two layer structure, a lower layer of the two layer structure comprising the same wiring material as gate electrodes of thin film transistors and , an upper layer of the two layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors".

Examiner disagrees with applicant and would like to present his point of view as follows:

First of all, Figures 5A-5B show the a driving circuit TFT ( which includes clock input terminals 208-209 in Figure 2 as well as clock input terminals 501-509 in Figure 6) formed in the same layers structure as a pixel TFT which includes gate, drain source (Figure 5B). Figure 6 further describes that "in the a driving circuit of a conventional liquid crystal display device, where clock wiring lines, video signal wiring lines, and control wiring lines of a shift register are formed, those wiring lines are formed at the same time a source and drain electrodes of a thin film transistor" (see page 5 line 24 through page 6, line 10 of the specification). Figures 4A- 4D clearly show at least two layers structure for forming source/drain and gate line electrodes. Figure 5A-5B show the wiring lines including clock lines (driver circuit TFT) associated with layers structure of source/drain gate line electrodes (i.e. pixel TFT). Furthermore, Figure 12B details of Figures 5A-5B how the clock lines or each of base portions of the clock lines is made of a two layer structure, a lower layer of the two layer structure comprising the same wiring material as gate electrodes of thin film transistors and , an upper layer of the two layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors. For example, the clock wiring lines are made of two layers: a lower layer (1114) is a gate electrode and an upper layer (1111, 1112) is a source and drain electrode.

While this is unlike applicant's disclosed device (Figure 12A), it reads on broad claimed language.

As to claims 10-12, 14-15, applicant argues that Figures 5 and 6 and Watanabe, either alone or combination, do not teach or suggest all that each of clock lines or each

Art Unit: 2675

of base portions of the clock lines is made of a two layer structure, a lower layer of the two layer structure comprising the same wiring material as gate electrodes of thin film transistors and , an upper layer of the two layer structure comprising the same wiring material as source and drain electrodes of the thin film transistors. However, this limitation is clearly taught by prior art admitted by applicant as previously discussed above. Applicant deleted a significant number of limitations issued in the parent application 09/150,930 (U.S. 6,281,865 B1) such as a first insulating substrate, black matrix, wiring lines, a second insulating substrate as well as wiring lines made of the same layer as the black matrices. Applicant now claims only the limitation two-layer structure which is so broad that it reads on the prior art. The claimed "two-layer structure" recited in the claims is not patentably distinct from the prior art admitted by applicant.

### ***Conclusion***

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

Art Unit: 2675

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

### **Inquiries**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chanh Nguyen whose telephone number is (703) 308-6603.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks


Washington, D.C. 20231


**or faxed to:**

**(703) 872-9306**

Hand-delivered responses should be brought to Crystal Park II, 2121  
Crystal Drive, Arlington, VA, Sixth Floor (Receptionist)

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

  
C. Nguyen  
August 17, 2004

  
CHANH NGUYEN  
PRIMARY EXAMINER